09/921561 PTO 08/06/01

Class	Subclass

ISSUE CLASSIFICATION

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
SCANNED TDR 8.A.	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/921561	F	~~365~~ 327	276	~~2812~~ 2816	M. Nguyen

APPLICANTS: Kazufumi Komura
Satoru Kawamoto

TITLE: Delay circuit, semiconductor integrated circuit device containing a delay circuit and delay method

PTO-2040 (12/99)

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)
INTERNATIONAL CLASSIFICATION			
			Continued on Issue Slip inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
The term of this patent shall not extend beyond the expiration date of _____	(Assistant Examiner)		(Date)		
	(Primary Examiner)		(Date)	ISSUE FEE	
				Amount Due	Date Paid
☐ The terminal ___ months of this patent have been disclaimed	(Legal Instruments Examiner)		(Date)	ISSUE BATCH NUMBER	

PTO-436A (Rev. 03/00)

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